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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/058,789 | 01/30/2002 | Masatoshi Kokubun | 100353-00095 | 4716 |

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| EXAMINER | |
|---|---|
| HANNETT, JAMES M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2622 | |

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/058,789 | KOKUBUN ET AL. | |
| | Examiner | Art Unit | |
| | James M. Hannett | 2622 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24 and 29-36* is/are pending in the application.

4a) Of the above claim(s) *5-10,15-24 and 31-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11-14,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments filed 3/30/2006n fully considered but they are not persuasive. The applicant has amended Claims 1 and 2 and argues that the prior art does not teach the new limitation that a transistor is provided between a drain of said first P-channel MOS transistor and a drain of said N-Channel MOS transistor to control a blooming of the CMOS sensor.

The examiner disagrees with the applicant. In the prior office action, the examiner relied upon transistor Q15 in Figure 15 to teach the claimed transistor for controlling blooming. However, the claim is written broadly and the examiner now views transistor Q13 and a first P-channel MOS transistor. The claimed an N-channel MOS transistor as transistor (Q15). Furthermore, the examiner views transistor (Q14) as the claimed transistor provided between a drain of said first P-channel transistor (Q13) and a drain of said N-channel MOS transistor (Q15). Furthermore, the entire voltage control circuit including all transistors (Q13-Q15) is used to control blooming. This new interpretation is necessitated by the amendment. Therefore, this action is Made Final.

The applicant should note that examiner **Brian Jelinek** is no longer the examiner assigned to this case. This action and all further actions will be addressed by Examiner **James M. Hannett**.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**1:** Claims 1-2, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,907,357 Maki in view of USPN 6,356,101 Erstad.

2: As for Claim 1, Maki discloses a CMOS sensor circuit (Fig. 10, PMOS transistor Q13 and NMOS transistor Q14) comprising: a photodiode (Fig. 10, diode sensor 40)., a reset transistor resetting said photodiode to an initial voltage (Fig. 10, reset transistor 45)., and a voltage control circuit controlling a gate potential of said reset transistor to a potential other than power source potentials (Fig. 3A, voltage rs controls the gate potential of the reset transistor to all potentials between a base voltage and Vdd), wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor (Fig. 15, inverter 12), the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal (Fig. 15, transistor Q13), an N-channel MOS transistor having a gate supplied with a second signal (Fig. 15, transistor Q15), and a transistor (Q14) provided between a drain of said first P-channel MOS transistor (Q13) and a drain of said N-channel MOS transistor (Q15) to control a blooming of the CMOS sensor circuit. However, Maki does not disclose a delay circuit producing said first signal by delaying said second signal.

Erstad discloses removing glitches from an inverter circuit using a delay Line (Figs. 1 and 2). One of ordinary skill in the art would have provided a delay Line in order to eliminate crow-bar current (col. 1-2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a delay circuit producing said first signal by delaying said second signal in order to eliminate crow-bar current.

3: In regards to Claim 2, Maki disclose a CMOS sensor circuit (Fig. 10, PMOS transistor Q13 and NMOS transistor Q14) comprising: a photodiode Fig. 10, diode sensor 40); a reset transistor resetting said photodiode to an initial voltage (Fig. 10, reset transistor 45); and a voltage control circuit keeping a gate potential of said reset transistor from completely becoming off (Fig. 4, the gate potential of the reset transistor is above the gate voltage of the read transistor, i.e. the reset transistor is never completely off; Fig. 3A, voltage rs controls the gate potential of the reset transistor to all potentials between a base voltage that is greater than zero and Vdd), wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor (Fig. 15, inverter 12), the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal (Fig. 15, transistor Q13), an N-channel MOS transistor having a gate supplied with a second signal (Fig. 15, transistor Q15), and a transistor (Q14) provided between a drain of and the first P-channel MOS transistor (Q13) and a drain of said N-channel MOS transistor (Q15) to control a blooming of the CMOS sensor circuit. Maki does not disclose a delay circuit producing said first signal by delaying said second signal.

Erstad discloses removing glitches from an inverter circuit using a delay Line (Figs. 1 and 2). One of ordinary skill in the art would have provided a delay line in order to eliminate crow-bar current (col. 1-2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a delay circuit producing said first signal by delaying said second signal in order to eliminate crow-bar current.

4: As for Claim 29, Erstad discloses the delay circuit is formed by an even number of inverters (Column 4, Line 27, the delay line is non-inverting.

5: In regards to Claim 30, Claim 30 is rejected for reasons discussed related to claim 29.

**6:** Claims 3, 4 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,907,357 Maki in view of USPN 6,356,101 Erstad in further view of USPN 5,768,203 Fuji.

7: As for Claim 3, Maki teaches a voltage control circuit (Figure 5) comprising: and inverter driving a gate of a reset transistor (Figure 5, Inverter 12), the inverter circuit including a first P-channel MOS transistor (Figure 5, transistor q13) and an N-Channel MOS transistor (Figure 5, transistor Q14); and a resistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor (Figure 5, resistor R). However, Maki does not teach the resistor may be configured as a transistor.

Fuji teaches a P-MOS transistor acts as a resistor when its gate and drain are connected (Column 5, Lines 64-66). One of ordinary skill in the art would have configured a resistor as a P-MOS transistor with its gate and drain connected because it is well known in the art that P-MOS transistors thus connected acts as a resistor (Column 5, Lines 64-66).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a resistor as taught by Fuji between a drain of the first P-channel MOS transistor and a drain of the N-channel MOS transistor as taught by Maki in view of Erstad because it was well known in that art that a P-MOS transistor with its gate and drain connected acts as a resistor.

8: In regards to Claim 4, Claim 4 is rejected for reasons discussed related to Claim 3.

9: As for Claim 11, Claim 11 is rejected for reasons discussed related to Claim 3.

10: In regards to Claim 12, Claim 12 is rejected for reasons discussed related to Claim 3.

11: As for Claim 13, Claim 13 is rejected for reasons discussed related to Claim 3.

12: In regards to Claim 14, Claim 14 is rejected for reasons discussed related to Claim 3.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Hannett whose telephone number is 571-272-7309. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
June 14, 2006

DAVID OMETZ
SUPERVISORY PATENT EXAMINER